A Multioctave Active GaAs MMIC Quadrature Phase Shifter

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Abstract—**A GaAs monolithic quadrature phase shifter based upon a phase locked loop system covers a 0.1 to 4.5 GHz frequency range. It provides about 8 dB of gain and its phase error and amplitude mismatch are respectively less than 2.5° and 0.4 dB over the band. When integrated into a single-sideband receiver, a sideband rejection of at least 30 dB has been achieved.**

I. Introduction

MANY SYSTEMS require a wide-band quadrature phase shift. One of the most important is the single-sideband radio receiver. In a classical hybrid approach, the signal at the image frequency is rejected by selective filters before mixing (Fig. 1(a)). The required quality factor of the resonator used in the filter is at least 30 and is often much more.

In state-of-the art MMIC's, the series resistance of inductive elements is of the order of 1 Ω/mm at frequencies up to a few GHz. At higher frequencies, it increases due to the skin effect. Consequently, at "low frequencies," the quality factor is much too low to achieve good rejection (in some systems the required level is 60–70 dB).

A way to overcome this drawback is to use an image rejection mixer (Fig. 1(b)). Two mixers are connected to the local oscillator via a quadrature splitter. The IF output signals are summed in a quadrature combiner, and the result is the addition of the IF voltages due to the desired input signal and the cancellation of those produced by the image frequency signal. The rejection is directly related to the quality of this cancellation, i.e., to the level of total (mixer plus combiner) amplitude mismatch ($\Delta A/A$) and phase error ($\Delta\varphi$):

$$\text{Rejection (dB)} = -6+10\log\left(\left(\frac{\Delta A_m}{A_m}+\frac{\Delta A_c}{A_c}\right)^2 + (\Delta\varphi_m+\Delta\varphi_c)^2\right). \quad (1)$$

Manuscript received July 13, 1989; revised August 24, 1989.

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IEEE Log Number 8931361.

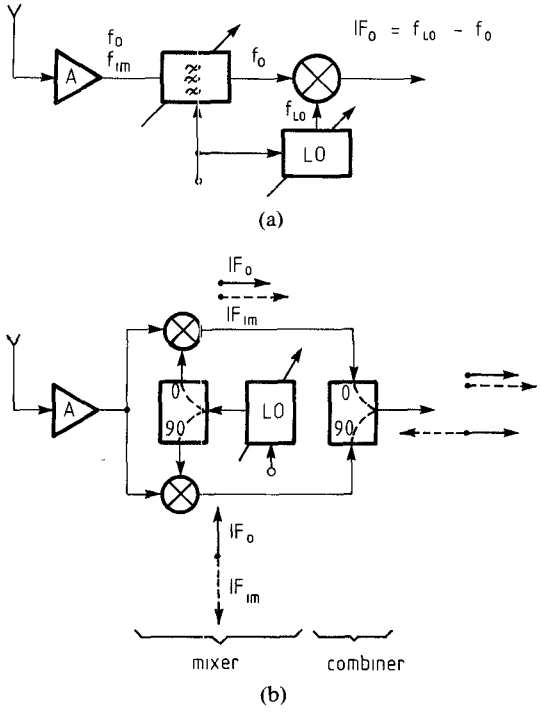

Fig. 1. Image rejection receivers. (a) Image frequency rejection before the mixing. (b) Image rejection mixer.

Fig. 2 shows the dependence of the rejection level on the amplitude and phase mismatches. We see that an accuracy of a fraction of a degree is required when a rejection of tens of dB is to be achieved.

As far as narrow-band receivers are considered, no major difficulties are anticipated for fabricating quadrature phase shifters. This is different when a wide frequency range, of many octaves, is to be covered. The bandwidth of the passive networks is too narrow, and they consume substantial substrate area at relatively low frequencies. The active phase shifters overcome this last drawback [1]. However, their relative bandwidth is still too limited.

In the application studied in our laboratory, the monolithic integration of a 0.1 to 4.5 GHz receiver, none of these solutions could be used. Therefore, we have resorted to an active system where a phase locked loop automatically forces the LO signals into phase quadrature [2]. The system (Fig. 3) consists of a voltage-controlled phase shifter (P), a quadrature phase comparator (C), and an integrator (I). The phase detector delivers a dc output signal when

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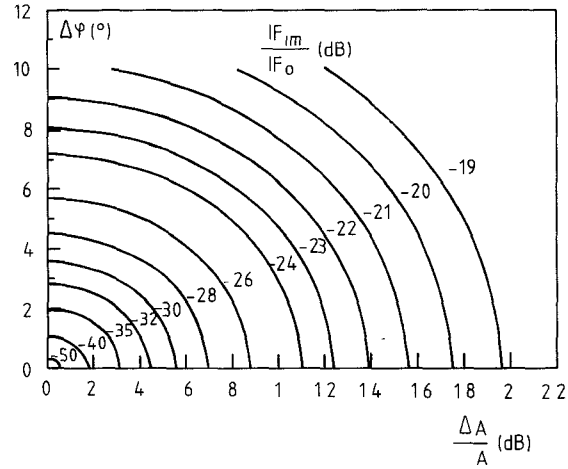


Fig. 2. Image frequency rejection as a function of the conversion gain mismatch of the two paths of mixer and phase error of quadrature phase shifters.

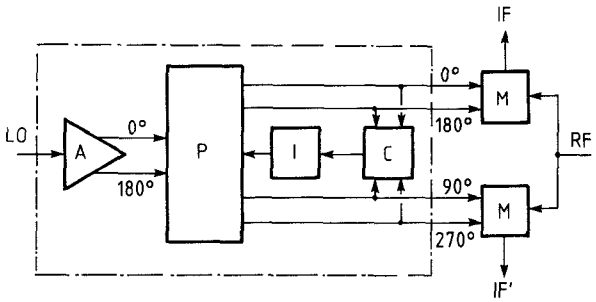


Fig. 3. Circuit diagram of LO quadrature phase shifter. A: input differential amplifier. P: voltage controlled phase shifter. C: phase comparator. I integrator.

the LO signal departs from quadrature. This error signal is integrated and fed back to the phase control input of the phase shifter. The system becomes stable when the integrator has zero input voltage, namely when quadrature is reached.

As double balanced mixers are used in the receiver, four quadrature signals are required. Therefore a phase splitter (A) is used at the input, which provides two 180° out-of-phase signals. It also performs the amplification of the LO signal.

II. Circuit Design

As the system is very wide band and "low frequency," no reactive matching is usable. At the very most, some inductive "help" at the upper end of the frequency range could be envisaged. However, since this is very inefficient in terms of real estate, we have avoided it.

Taking into account the complexity of the circuit, we chose, despite a lower f_t, a 0.7 μm process for its higher fabrication yield.

A. Voltage-Controlled Phase Shifter

A RC all-pass network (Fig. 4) is used as a phase shifter. The quadrature phase shift occurs when $\omega R_p C_p = 1$. This condition is met by varying the channel resistance of a MESFET with zero drain bias. As long as the peak

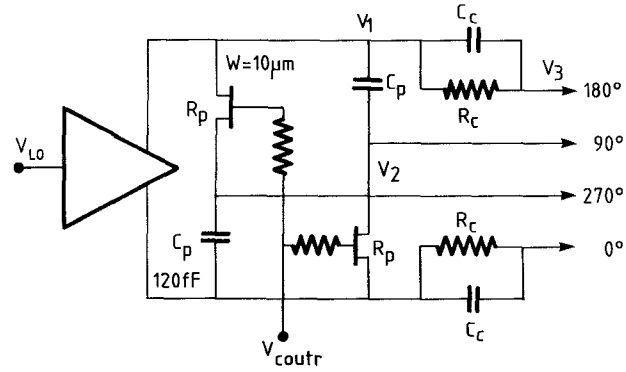


Fig. 4. Voltage-controlled phase shifter.

drain-to-source voltage is lower than the saturation voltage, the MESFET behaves as a linear resistor, its value being controlled by the gate voltage.

The phase shifter relative bandwidth is limited mainly by the maximum-to-minimum resistance ratio. The minimum resistance is roughly equal to V_{sat}/I_{max} where V_{sat} is the saturation voltage and I_{max} the maximum saturated drain current. The maximum resistance is not so well defined. The leakage drain-to-source resistance can be very high when the FET is pinched off, but the linearity requirements limit the maximum useful resistance to a somewhat lower value. Practically, the useful resistance ratio is of the order of 50–100.

The value of C_p (and implicitly of R_p) is the result of a trade-off between two contradictory requirements. One is that the impedance of the $R_p - C_p$ all-pass network must be high compared to the output impedance of the driving stage in order to achieve a high cutoff frequency. At the frequency f_q for which the quadrature phase shift is achieved, the inpedance Z_q of the all-pass network is

$$Z_q = \frac{1-j}{4\pi f_q C_p} \tag{2}$$

and the 3 dB cutoff frequency f_c of the driving amplifier loaded by the all-pass network is given by

$$f_c = \frac{\sqrt{3}-1}{4\pi R_{out} C_p} \tag{3}$$

where R_{out} is the differential output impedance of the driving amplifier. For a reasonable power consumption, R_{out} is limited to about 100 Ω. To achieve a cutoff frequency of at least 4.5 GHz, we deduce from (3) that

$$C_p \leqslant 130\, fF. \tag{4}$$

The other requirement is that C_p must be high compared to the input capacitance C_{in} of the following stage in order to minimize the amplitude mismatch between the phase shifter outputs. The phase-shifted voltage V_2 of the all-pass network is related to the input reference voltage V_1 by

$$\frac{V_2}{V_1} = \frac{1 - j\omega R_p C_p}{1 + j\omega R_p (C_p + C_{in})}. \tag{5}$$

When the phase shift is 90°, the attenuation is given by

$$\left|\frac{V_2}{V_1}\right| = \sqrt{\frac{1}{1+C_{in}/C_p}}. \tag{6}$$

Fortunately, as the mixers operate in saturation, their conversion gains do not vary significantly with the local oscillator level. Assuming a 0.1 dB change in conversion gain for a 0.4 dB change in LO level, the LO amplitude mismatch has to be lower than 0.2 dB in order to achieve 50 dB of image rejection. From (6) we deduce that

$$C_{in} \leqslant 20C_p. \tag{7}$$

Taking into account the upper limit of C_p given by inequality (4), inequality (7) limits the input capacitances C_{in} to less than 10 fF. Such a low input capacitance is almost impossible to achieve. Therefore we introduced a compensation circuit which can attenuate the 0/180° signals exactly with the same ratio as (5), independently of the frequency or the phase shift [4]. Its transfer function is given by

$$\frac{V_3}{V_1} = \frac{1+j\omega R_c C_c}{1+j\omega R_c(C_c+C_{in})}. \tag{8}$$

If $C_c = C_p$ and $R_c = R_p$, the amplitude mismatch is exactly compensated. However, even for a constant R_c value, equal to R_p in the center of the frequency band, the amplitude mismatch is greatly reduced. Thus, due to the compensation circuit, the input capacitance of the mixer can be much higher than the value given by inequality (7).

The CAD simulation of the complete voltage-controlled phase shifter showed a nearly linear dependence of the frequency f_q on the control voltage V. The slope df_q/dV is about 1.3 GHz/V. The slope of the phase variation with frequency is $(\partial\varphi/\partial f)_{f_q} = 1/f_q$, and the quadrature phase shifter voltage sensitivity S_v is

$$S_v = \frac{\partial\varphi}{\partial V} = \frac{1}{f_q}\cdot\frac{df_q}{dV}. \tag{9}$$

The sensitivity decreases with frequency as $1/f$ and is about 75°/V at 1 GHz.

B. Phase Detector

The performance of the system is largely dependent on the quality of the phase detector. It is basically a multiplier, delivering a dc output signal proportional to the cosine of the phase difference between the two input signals.

It is essential in the phase detector to avoid any dc signal that does not arise from a phase difference. One of the main source of dc parasitics in a detector with symmetrical outputs is a biasing voltage unbalance. To avoid it, a zero biased structure has been used (Fig. 5). It consists in two parallel double balanced ring multipliers, each composed of four FET's behaving as voltage-controlled resistors. The symmetry of this structure ensures identical loading of the four outputs of the phase shifter.

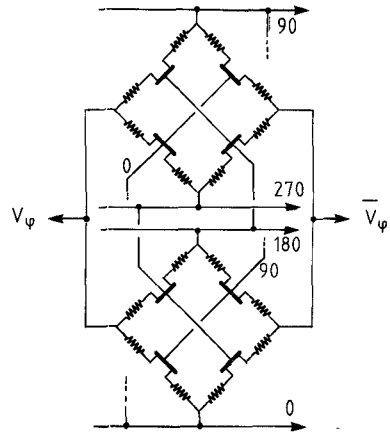


Fig. 5. Double balanced phase comparator.

A second source of parasitic dc output signal is the signal distortion. To avoid it, the peak drain-to-source voltage must be lower than the FET saturation voltage. In order to meet this requirement, we have added a series resistance to the FET's, although it decreases the sensitivity of the phase detector. Other solutions could have been used, such as increasing the gate length in order to increase the saturation voltage.

Another reason to choose a passive structure is that the low-frequency noise is much lower than in an active one, since no dc current flows through the transistors. The amplification of this noise via the loop integrator with high dc gain could generate phase noise or even lead to loop instability.

The phase sensitivity S_φ of the phase detector depends on the amplitude A of the input signals:

$$S_\varphi = KA^2 \tag{10}$$

where K is a constant characterizing the detector. For LO signal of about 1 V peak, the sensitivity is approximately 7 mV/° up to 3 GHz. It decreases down to 2 mV/° around 4.5 GHz as the phase shifter gain and therefore the LO signal decrease.

C. Mixers

Two active double balanced mixers are included in the circuit (Fig. 6). Due to the balanced configuration, the LO signal is rejected at the drain of the six transistors that compose the basic mixer. In this way, there is no contribution of the drain nonlinearities to the intermodulation distortion, and a third-order input intercept point as high as 15 dBm is achieved.

The basic mixer is matched to 50 Ω by an output buffer stage; it is a balanced push–push amplifier. Assuming that the signals at the inverting and noninverting inputs are of equal amplitude but opposite phase, the voltage gain A_v of the push–push stage at low frequency is given by

$$A_v = \frac{2g_m}{Y_0 + g_m + 2g_d} \tag{11}$$

where g_m and g_d are respectively the transconductance and the output conductance of the transistor, and Y_0 is the

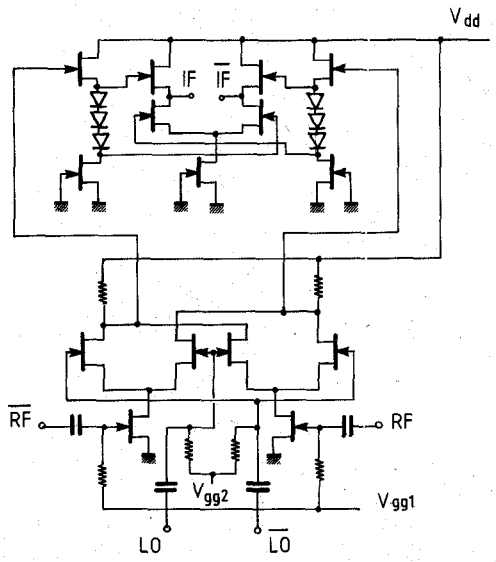


Fig. 6. Double balanced mixer.

load admittance. The gain provided is 6 dB more than that provided by a conventional common-drain buffer.

The transistor sizes of the three-stage mixer (basic mixer, intermediate buffer, and output push–push stage) have been optimized to obtain the best trade-off between noise figure and current consumption.

III. Fabrication

The monolithic circuit (Fig. 7) containing the complete quadrature phase shifter (except the integrator) and the two double balanced mixers has been processed at the Philips Microwave Foundry in Limeil-Brévannes, France, using the DO7A process. The main features of this process are a 0.7 μm gate length, a threshold voltage of -3 V, a second level of metallization on SiO_2, and an absence of via holes.

The circuit contains 86 FET's ranging from 8 μm to 120 μm gate width, of which 30 belong to the mixers. Its size is about 1×2 mm^2. Despite the circuit complexity, the RF yield was more than 60 percent.

IV. Measurements

Since the circuit is intended to be used in a broad-band radio receiver, the most natural way to evaluate the circuit performance is to perform image frequency rejection measurements. It is also the most accurate method because it emphasizes very low phase errors and amplitude mismatches that cannot be measured directly. To perform image rejection, an external IF quadrature combiner is required. In order to minimize as much as possible the contribution of the combiner to the limitation of the image rejection level, we operate at an IF frequency for which the combiner has simultaneously low phase error and low amplitude mismatch. An IF frequency close to 30 MHz is chosen, for which $\Delta\varphi_c = 0.5°$ and $\Delta A_c = 0$.

The open-loop operation of the circuit has been tested first. Fig. 8 shows the output voltage of the phase detector as a function of the phase shifter control voltage at three

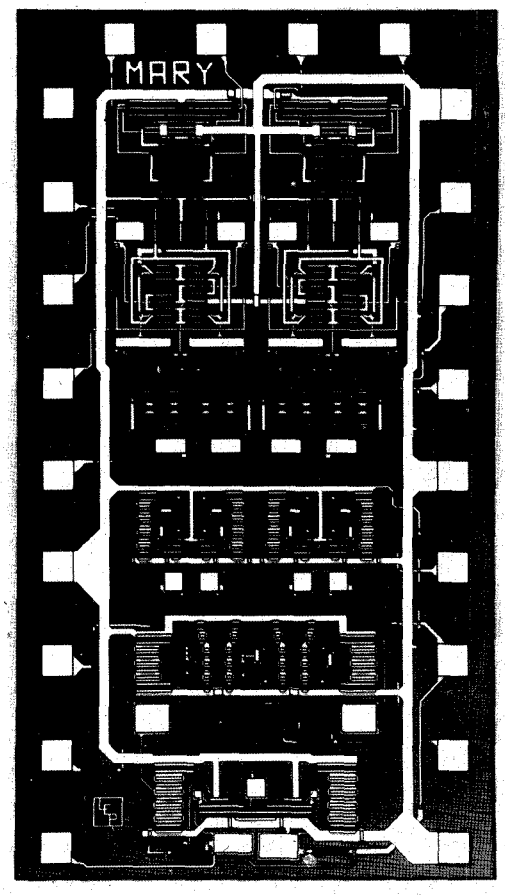


Fig. 7. Microphotograph of the MMIC. Overall dimension are 1×2 mm^2.

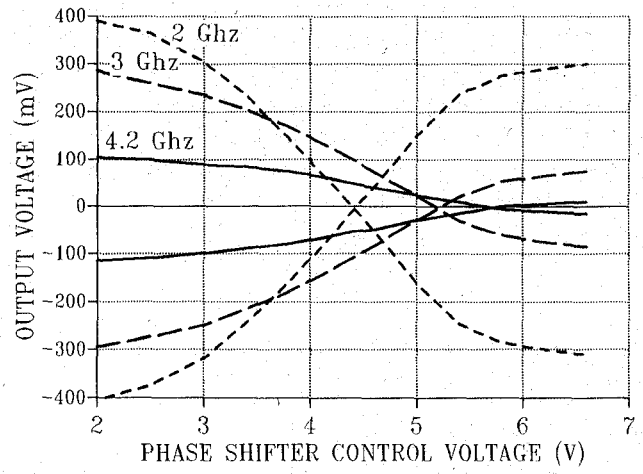


Fig. 8. Phase detector output characteristic.

LO frequencies. The outputs are nearly perfectly symmetrical and the dc offset is very low ($\leqslant$10 mV). Since the resistance R_p of the all-pass network decreases when the control voltage increases, the quadrature condition ($\omega R_p C_p = 1$) is met at a higher control voltage as the frequency increases. As expected, a decrease in sensitivity is observed when increasing the frequency. Fig. 9 shows the image rejection level measured at 2 GHz as a function of the control voltage. The rejection is maximum nearly exactly when the phase detector output is zero, showing the correct behavior of the phase detector. The maximum rejec-

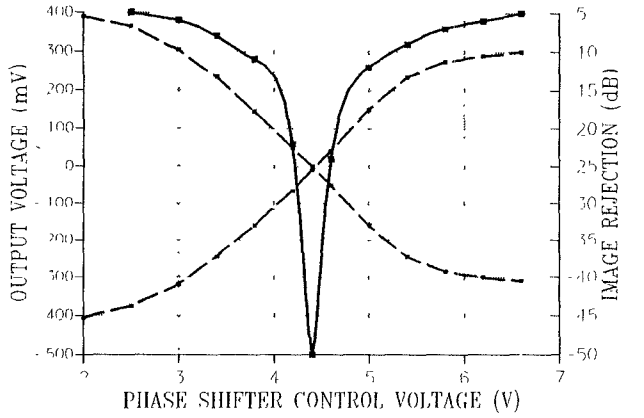


Fig. 9. Open-loop operation. Measured phase comparator output voltage and image frequency rejection versus phase shifter control voltage: $f_0 = 2$ GHz.

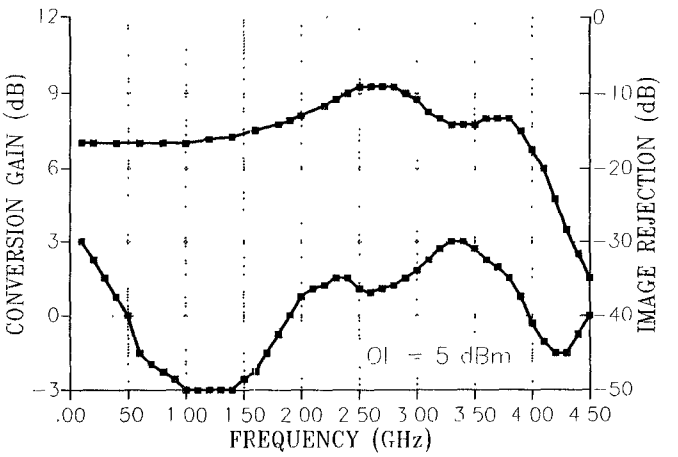


Fig. 10. Locked loop operation. Measured conversion gain and image frequency rejection versus frequency.

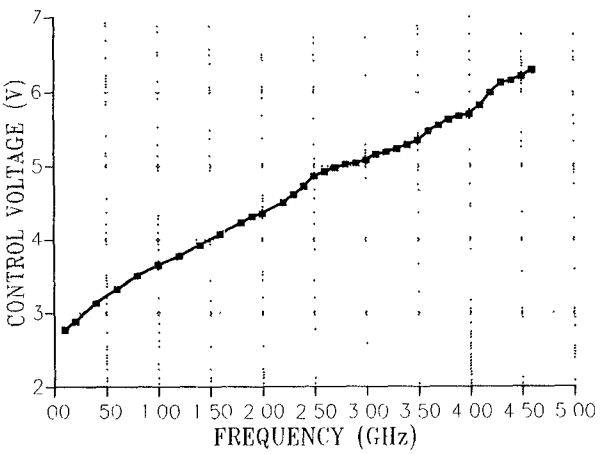


Fig. 11. Locked loop operation: measured phase shifter control voltage at the output of the integrator versus frequency.

tion occurs when the phase errors of the circuit and the combiner compensate each other ($\Delta\varphi_m + \Delta\varphi_c = 0$). The 50 dB maximum rejection level means that the amplitude mismatch $\Delta A_m/A_m$ between the mixer outputs is about 0.05 dB.

The quadrature phase locked operation requires a loop amplifier that feeds back the error signal to the voltage-controlled phase shifter. The static phase error $\Delta\varphi_m$ of the closed-loop system is related to the dc gain A_0 of the amplifier and to the sensitivities S_v and S_φ of the voltage-controlled phase shifter and the phase detector respectively by the following expression:

$$\Delta\varphi_m = \frac{S_v V_0}{1 + A_0 S_v S_\varphi} \simeq \frac{V_0}{A_0 S_\varphi} \tag{12}$$

where V_0 is the control voltage to which corresponds a phase shift of exactly 90° at the frequency of operation. As V_0 increases with the frequency while the phase detector sensitivity decreases, the phase error increases quite rapidly with the frequency. Taking into account the above values of V_0 and S_φ, a dc gain A_0 of at least 5000 is required to limit the phase error to about 1^0 at 4.5 GHz. To achieve such a high gain, we use an external amplifier.

When locking the loop, the system always stabilizes in quadrature condition regardless of the frequency. Similar good behavior is observed in response to a change of the LO frequency. The response time has not been measured since the system is intended for static operation. It is mainly limited by the frequency bandwidth of the loop amplifier.

Fig. 10 shows the conversion gain of the system and the image rejection level as a function of the LO frequency. The gain is about 8 ± 1 dB up to 4 GHz and decreases rapidly at higher frequencies, mainly because of a lower LO signal amplification through the phase shifter. The rejection level is at least 30 dB over the 0.1–4.5 GHz frequency band and is as high as 50 dB around 1 GHz. Sharing equally the causes of the finite rejection between phase error and amplitude mismatch, we can calculate according to expression (1) that $\Delta A/A \leqslant 0.4$ dB and $\Delta\varphi \leqslant 2.5°$ over the frequency band.

Fig. 11 shows that the band is covered with about 3.5 V variation of the control voltage delivered by the loop integrator. As expected, the control voltage increases almost linearly with frequency.

V. Conclusion

A phase locked loop technique has been used for the first time in the implementation of a broad-band MMIC quadrature phase shifter. Compared to other passive or active approaches, this technique has the advantage of combining high phase precision with broad-band capability. It has been successfully demonstrated within a radio receiver which has achieved at least 30 dB of image rejection over a 0.1–4.5 GHz frequency band. The achievement of such a result requires a very low dispersion between components within a circuit and is therefore a good demonstration of the present maturity of GaAs technology. Finally, our results also show that design methods based on voltage amplification instead of power amplification, without any impedance matching between stages, can be extended up to the microwave domain since GaAs

devices currently have an f_t of the order of 20 GHz or more.

ACKNOWLEDGMENT

The authors take this opportunity to thank their colleagues from the Philips Microwave Foundry for the fabrication of the circuits.

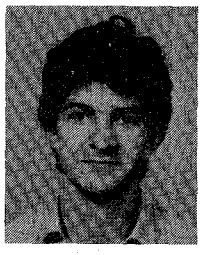
REFERENCES

[1] S. K. Altes, T. H. Chen, and L. J. Ragonese, "Monolithic *RC* all-pass networks with constant-phase-difference outputs," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-34, pp. 1533–1537, Dec. 1986.

[2] S. R. Al-Araji and W. Gosling, "A direct conversion VHF receiver," *Radio Electron. Eng.*, vol. 43, no. 7, pp. 442–446, July 1973.

[3] P. Jean, V. Pauker, and P. Dautriche, "Wide-band monolithic GaAs phase detection for homodyne reception," in 1987 *IEEE MTT-S Int. Microwave Symp. Dig.*, (Las Vegas), pp. 169–171.

[4] P. Philippe, French patent 89.07441.



Pascal Philippe was born in France on August 28, 1959. He received the Docteur es Sciences degree in 1985 from the Université des Sciences et Techniques de Lille, France, for his work on optoelectronics in the Laboratoire Central de Recherche (Thomson CSF), Orsay, France.

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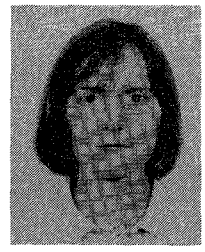

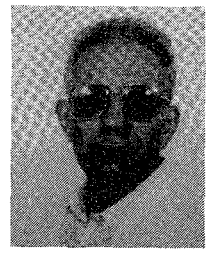

Vlad Pauker (SM'89) received the M.S. degree in electronic engineering from Bucharest Polytechnical Institute in 1952 and the Ph.D. degree in 1957.

In 1957, he became a research scientist at the Institute of Nuclear Physics of the Rumanian Academy of Science. From 1956 to 1958, he was an Assistant Professor at the Bucharest Polytechnical Institute. In 1960, he founded the Solid State Device Application Laboratory of IPRS (Bucharest). In 1969, Dr. Pauker joined RTC in Paris, leading the development of solid-state microwave circuits. Since 1979, he has been working at LEP, Paris, where he now supervises the study of GaAs microwave monolithic integrated circuits.

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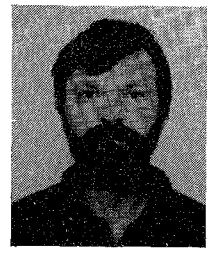
In 1983, he joined the Laboratoires d'Electronique et de Physique Appliquée, Limeil-Brévannes, France, to work on GaAs analog IC's and, more particulary, on the design of integrated receivers. In 1987, he joined Thomson Military and Space Components to work on the design of high speed CCD sensors.



Patrick Jean was born in France in 1961. From 1984 to 1987, he worked at LEP (Laboratoires d'Electronique Philips) for TRT (Télécommunications Radioélectriques et Téléphoniques), where he designed a wide-band integrated double balanced mixer. Since 1988, he has been with TRT, where he is involved in MMIC design. He received the Doctor degree (Thèse de Doctorat) in "Communications Optiques et Microondes" from the University of Limoges in 1989.